Code ..... **Course item: .....**

1. INFORMATION ABOUT THE COURSE

A. Basic information

Name of course	***Digital Circuits***
Study level	*First degree*
Unit running the study programme	*Faculty of Telecommunication, Computer Science and Electrical Engineering*
Study programme	*Electronics and Telecommunications*
Speciality	
Name of teacher (s) and his academic degree	*Damian Ledziński, Ph.D., Piotr Grad Ph.D.*
Introductory courses	*none*
Prerequisites	*no prerequisites*

B. Semester/week schedule of classes

Semester	Lectures	Classes	Laboratories	Project	Seminars	Field exercises	ECTS
winter or summer			30				4

2. EFFECTS OF EDUCATION (acc. to National Qualifications Framework)

Knowledge	*on successful completion of the course student is supposed to define and solve any specific problem from digital circuits area*
Skills	*on successful completion of the course student is supposed to analyse any specific problem from digital area, formulate any problem on abstractive level, solve defined problem and implement it in FPGA technology.*
Competences	*on successful completion of the course student is supposed to be able to cooperate with the other students to solve specific digital problems.*

3. TEACHING METHODS

laboratory

4. METHODS OF EXAMINATION

projects during laboratories lecture

5. SCOPE

Lectures	
Laboratories	*Introduction to digital circuits. Some example. Axioms and rules of Boolean algebra. Boolean functions. True tables. Functionally complete systems. Specification of logical functions. Combinational circuits. Formalization of the description. Basic gates. NAND and NOR gates. XOR gates. Algebraic minimization of logical expressions. Fundamentals of mnemonic methods of*

	minimizing logical functions. Minimization of logical functions using Karnaugh maps. Don't care values. Sum of Products normal form. Product of Sums normal form. Quine and McCluskeys method of minimization. Static and dynamic hazards. Combinational circuits utilizing multiplexers. Combinational circuits utilizing decoders and demultiplexers. Combinational circuits utilizing read only memory. Design exercises. Synchronous circuits. General introduction. Problem formulation. Automaton state. Graphs. State transition and output table. State transition and output table. Partial equivalence of Moore and Mealy automatons. Coding. D, T, JK, RS flip flops. Flip-flop excitation tables. Synchronous automaton realization. Equivalence of complete (fully specified) automaton states. Compatibility of incomplete Laboratories *(partially specified) automaton states. Formalization of the minimization algorithms. Realization of a minimal automaton using D, T, JK, RS type flip-flops. Design exercises. Asynchronous circuits. Fundamentals of asynchronous circuit design. Time plots. Assigning of states. Primary state transition and output table. Minimization of the number of states. Races. State coding. Cyclic transitions. State coding using hypercubes. Coded state transition and output table and the realization of the automaton. Method of minimizing asynchronous automatons. An example of the utilization of the alternative method of minimizing asynchronous automatons. Asynchronous circuit design using state graphs. Problem formulation. Creation of the state graph. Minimization of the number of states and coding. Realization of an automaton. Design exercises.*

6. **LITERATURE**

Basic literature	*Sasao T., 1999. Switching Theory for Logic Synthesis. Springer*
Supplementary literature	*Hassoun S., Sasao T., 2001. Logic Synthesis and Verifications. Springer.*